PRE-ERASE MANUFACTURING METHOD

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BACKGROUND OF THE INVENTION

[0001] Production of structures on a die section of a wafer typically involves plasma or reactive ion etching. These and other anisotropic etching methods are among production steps that can result in a charge accumulation. Charge accumulation can cause unstable device characteristics and low yield, particularly for non-volatile memories. Conventionally, exposure to UV radiation before division of the wafer into dies has been used to relieve the charge accumulation. Exposure to UV radiation is not a universal remedy, as some memory structures and materials accumulate charges, instead of relieving them, when exposed to UV.

[0002] Accordingly, an opportunity arises to devise methods that relieve charge accumulation from structures on the die sections of a wafer, during manufacturing, without UV exposure.

SUMMARY OF THE INVENTION

The present invention includes methods to pre-erase non-volatile memory cells using an electrical erase signal prior to dividing a wafer into dies. Particular aspects of the present invention are described in the claims, specification and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] **FIG. 1** is a flow chart of a traditional testing and wafer sorting process.

[0004] **FIG. 2** is a flow chart of a pre-erase step, added to traditional testing and wafer sorting.

[0005] **FIG. 3** is a flow chart of a pre-erase step and a bake step added to traditional testing and wafer sorting.

[0006] **FIGS. 4A-4B** are schematic diagrams of memory cells.

DETAILED DESCRIPTION

[0007] The following detailed description is made with reference to the figures. Preferred embodiments are described to illustrate the present invention, not to limit its scope, which is defined by the claims. Those of ordinary skill in the art will recognize a variety of equivalent variations on the description that follows.

[0008] **FIG. 1** is a flowchart of wafer processing during the so-called sort. Between the start **101** and end **131** of the sort, various tests are performed, which may include DC tests **121** and AC tests **122**. Conventional tests may include testing for open or short conditions and column or word line stress tests. The outcome of these tests determines how the wafer will be further processed. For instance, the wafer may be scrapped, it may go through additional process steps or it may be subdivided into dies and packaged as chips (so-called back end processing.)

[0009] One of the outcomes of sorting is to detect unstable or defective circuits in dies. In some fabs, if more than half of the dies tested (e.g., 3 of 5 dies) are defective, the wafer is scrapped. For non-volatile memories, a cause of unstable, non-uniform or defective circuits is charge accumulation in memory cells. Non-volatile memories depend on charges preserved in a layer or gate. In a floating gate arrays, for instance, an accumulation of charges during production can make a cell unusable. ONO structures, for instance, are vulnerable to trapping of charges in the nitride layer during manufacturing. The vulnerability of the nitride layer is apparent in production of NROM and in application of SONOS and MONOS manufacturing processes.

[0010] Build up of electrical charges during anisotropic etching is a well-known phenomena. Charges from plasma, reactive ions or other substances used for etching are particularly attracted to some layers, such as metal layers. One of the phenomena is an antenna effect, in which certain patterns of metal in a layer accumulate a substantial charge that can damage memory cells in many ways, including burning through layers during a discharge or being trapped in a layer that is supposed to be programmable.

[0011] Charge build up during manufacturing is neutralized in some manufacturing processes by exposure of partially completed wafers to UV. Erasable UV-EPROMs have been in use for a long time, giving way recently to EEPROMs. Unfortunately, this is not a universal solution to charge build-up, because UV exposure increases charge accumulation for some processes and some structures,

instead of relieving it. Pre-erasing using an electrical erase signal offers an alternative to UV exposure, during manufacturing.

[0012] **FIG. 2** depicts addition of a pre-erase step **211** prior to testing **121, 122** of the dies on a wafer. The exact placement of this pre-erase step is not critical to this invention, but illustrates of the usefulness of improving wafer and die yield prior to determining whether the dies are defective. Preferably, the pre-erase step takes place after the last step that produces substantial charge accumulation in a memory layer. This may be very late in the process, after a passivation layer has been applied and after pads have been exposed by etching. Or, for a memory cell that is buried, pre-erase may take place after covering whatever metal layers are directly above the memory cell. These metal layers may be covered by an insulating layer or a passivation layer. The pre-erase step can take place at any point in the process before the wafer is subdivided into dies.

[0013] A pre-erase step can be carried out in virtually any way that an electrical erase ordinarily is performed on a non-volatile memory cell. The patent literature is very rich in examples of erasure strategies. One erasure process that may be used is a negative gate channel erase. This erase functions by Fowler-Nordheim tunneling. **FIGS. 4A-4B** identify regions that may be charged during an erasure in a floating gate and NROM or similar memory structure, respectively. A negative gate channel erase involves applying a voltage Vg to the control gate **401** and an opposite voltage Vs, Vb to the source **411** and the bulk or substrate **412** in the channel region. The drain **413** voltage Vd is allowed to float in this erase mode. In this erase and the others that follow, the functions of the drain and source can be reversed, with the opposite voltage applied to the drain and the source allowed to float. The source and drain can generically be referred to as two terminals for erasure purposes. One set of useful voltages for this erase is Vg = -12v, Vs=Vb=8v and Vd floats. Another erasure process that may be used is a negative gate source side erase. This erase functions by Fowler-Nordheim tunneling. A negative gate source (or drain) side erase involves applying a voltage Vg to the control gate **401** and an opposite voltage Vs to the source **411.** The bulk or substrate **412** in the channel region is grounded to 0v. While the bulk in these illustrations appears to be a substrate, it may be a doped channel or an isolated doped channel, e.g., one surrounded by a further doped channel of an opposing doping type. The drain **413** voltage Vd is allowed to float in this erase mode. One set of useful voltages for this erase is Vg = -8v, Vs=6v, Vb=0v and Vd

floats. In this erase, the functions of the drain and source can be reversed, with the opposite voltage applied to the drain and the source allowed to float. A further erasure process that may be used is a hot hole erase. This erase functions by injecting holes into the cell. Two variations on the hot hole erase apply voltages to one or both of the source and drain. In one variation, a hot hole erase involves applying a voltage Vg to the control gate **401** and an opposite voltage Vs to the source **411.** The bulk or substrate **412** in the channel region is grounded to 0v. The drain **413** voltage Vd is allowed to float in this erase mode. One set of useful voltages for this erase is Vg = -3v, Vs=8v, Vb=0v and Vd floats. In this erase, the functions of the drain and source can be reversed, with the opposite voltage applied to the drain and the source allowed to float. Another variation involves biasing both the source and drain, instead of allowing one to float. Injection of hot holes into a floating gate **402** or an ONO layer **422** relieves build up of electrons, which may be difficult to extract.

[0014] **FIG. 3** adds an additional bake **311**, following the pre-erase **211**. This bake should be under conditions sufficient to diffuse charges added to the floating gate **402** or the ONO layer **412** by the erase. Two different temperature ranges appear to be useful: 80-150 degrees Celsius and 150-250 degrees Celsius. The time required for sufficient effect can readily be determined, without an excessive degree of experimentation.

[0015] Not illustrated but useful with the present invention is a verify step to determine the erasure state of memory cells. Many verification and correction schemes have been described for non-volatile memory and particularly for EEPROM or NROM memories. Virtually any of them can be used with the present invention, if enough time is allowed during processing. The general scheme is that if a memory cell with an improper erasure state is found, a further signal is sent to alter the memory cell. In some instances, the desired charge is deliberately under achieved, so that it will not be exceeded with corrective signals. In other instances, over achieving is allowed, either with or without correction. In connection with the present invention applied to an NROM cell, a surplus of holes may be better than a surplus of electrons, as the subsequent programming process accumulates electrons.

[0016] While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which

modifications and combinations will be within the spirit of the invention and the scope of the following claims.

[0017] We claim as follows: